Potential induced degradation of pre-stressed photovoltaic modules
Influence of polarity, surface conductivity and
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Potential Induced Degradation of Pre-stressed Photovoltaic Modules: Influence of Polarity, Surface Conductivity and Temperature

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Abstract — Potential induced degradation (PID) is one of the factors that could contribute to the long-term degradation of PV modules. It is, therefore, essential to carry out the PID test for different open-air conditions as well as both voltage polarities for modules that maybe designated by the manufacturer to operate in either polarity. This paper evaluates the influence of PID test temperature, humidity-based and carbon-based surface conductivity of glass, and system voltage polarity on the degree of PID effects on fresh and pre-stressed (thermal-cycling or damp-heat) mono- and poly-crystalline silicon modules. Irrespective of PID test temperature (85°C or 60°C) and pre-history (fresh or pre-stressed in damp-heat or thermal-cycling), this work indicates that the positive-voltage has little or no PID effect on all the tested modules when humidity or carbon is used for the glass surface conductivity. In contrast, irrespective of PID test temperature (85°C or 60°C) and pre-history (fresh or pre-stressed in damp-heat or thermal-cycling), all the tested modules appear to be susceptible to the negative-voltage when conductive carbon (carbon layer) is used for the glass surface conductivity. However, when humidity is used for the surface conductivity instead of carbon, only the fresh and damp-heat stressed modules, excluding thermal-cycling stressed modules, appear to be susceptible to the negative voltage irrespective of PID test temperature (85°C or 60°C). It is also concluded that the humidity based approach may be a better replication of the field degradation (if any) pattern as compared to the metallic/carbon conductive layer approach.

Index terms — durability, potential induced degradation, reliability, system voltage, leakage current

I. INTRODUCTION

High system voltage (600-1500V) in the PV systems could lead to leakage of current from the active circuit to the ground and hence could cause durability issues (called potential induced degradation, PID) with slow degradative losses depending on the polarity and magnitude of leakage current. The PID effect can be increased by increasing applied/system voltage, increasing operating temperature and/or increasing an electrical conductivity between active circuit and module frame through module surface conductivity (for example, condensed water layer on the glass surface), interfacial conductivity (for example, between cell and encapsulant) and/or bulk conductivity (for example, through encapsulant). Therefore, the lack of a system voltage durability test and understanding of the crystalline silicon modules under high voltage in open air conditions could be detrimental to the long-term durability of the system.

A very high surface conductivity layer of carbon extending all the way from the glass surface to the frame was used in our previous study [1]. In reality, this type of high surface conductivity in the field condition could happen only on sunny/cloudy days during heavy salt-loaded (marine/costal conditions) rains. Therefore, it was decided to continue the previous study but with lower surface conductivity layers or methods in order to better simulate the field conditions.

In the current study, the influence of temperature (60°C and 85°C) and lower surface conductivity humid/water film on PID is investigated at the system voltages of +600V and -600V. In previous studies reported by other research groups, fresh unstressed modules have been subjected to the PID evaluations [2, 3]. The PID effect may depend on the prior accelerated-stress history (fresh, damp-heat or thermal-cycling) or the actual-field history of the modules. This study compares the influence of module’s prior accelerated-stress history on the magnitude of PID losses.

II. METHODOLOGY

The PV modules which were evaluated in this study had three prior histories: damp-heat (DH1000) tested modules according to IEC 61215 standard [4]; thermal-cycling (TC200) tested modules according to IEC 61215; non-stressed fresh (control) modules. In our previous study [1], the conductive carbon-layer was applied on the glass surface of the module to obtain surface conductivity by maintaining 85% relative humidity inside an environmental chamber. As shown in Table I, the experiments were devided into 4 projects (four manufacturers: mf2, mf3, mf4, mf8). Each project consists of either 4 or 5 modules.

In all the four projects, the relative humidity (85%RH) and applied voltage (600V) were kept constant. The effects of polarity (positive or negative) and temperature (60°C or 85°C) were investigated in the first three projects. In order to investigate and confirm the repeatability of the effect of temperature, the modules from the fourth project (mf8) were used, and their test results are not discussed here. The carbon-based results presented in this paper (referred as
are based on the previous publication [1] and they are compared with the humidity-based results obtained in the current study.

<table>
<thead>
<tr>
<th>Project</th>
<th>Technology</th>
<th>Coated Module</th>
<th>TC 200-1</th>
<th>DH1000-1</th>
<th>TC 200-2</th>
<th>DH1000-2</th>
<th>Total</th>
</tr>
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<tbody>
<tr>
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<td>Mono-Si</td>
<td>0012</td>
<td>0003</td>
<td>0005</td>
<td>0004</td>
<td>0008</td>
<td>5</td>
</tr>
<tr>
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<td>0009</td>
<td>0008</td>
<td>0004</td>
<td>0002</td>
<td>NA</td>
<td>4</td>
</tr>
<tr>
<td>mf3</td>
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<td>0769</td>
<td>0764</td>
<td>0759</td>
<td>0717</td>
<td>5</td>
</tr>
<tr>
<td>mf4</td>
<td>Poly-Si</td>
<td>0023</td>
<td>0024</td>
<td>0002</td>
<td>NA</td>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

The experimental setup used for this PID investigation is shown in Figure 1. As shown in the flow diagram of Figure 2, the test plan was executed on eighteen mono- and poly-crystalline silicon modules in 3 phases:

- **Phase-I: Positive Bias**
  - Apply +600V to cell active circuit
  - Maintain the chamber condition at 85°C/85%RH or at 60°C/85%RH
  - Characterize the modules at, typically, every 5-hour PID cycle
  - Apply PID stress for 35 hours (7 cycles)

- **Phase-II: Negative Bias**
  - Apply -600V to cell active circuit
  - Maintain the chamber condition at 85°C/85%RH or at 60°C/85%RH
  - Characterize the modules at, typically, every 5-hour PID cycle
  - Apply PID stress for 35 hours (7 cycles)

- **Phase-III: Regeneration/Recovery Bias**
  - Apply +600V to cell active circuit
  - Maintain the chamber condition at 85°C/85%RH or at 60°C/85%RH
  - Characterize the modules at, typically, every 5-hour PID cycle
  - Apply PID stress for 35 hours (7 cycles)

A variety of diagnostic tools and instruments were used for the pre- and post-test characterizations of the modules. They include: Electroluminescence imaging, infrared imaging, visual inspection, light I-V and dark I-V.

### III. RESULTS AND DISCUSSION

The prior research work on PID at ASU-PRL was conducted at the positive and negative voltage biases of 600V at 85°C with no humidity but with carbon conductive coating applied to the glass superstrate contacting module frame [1]. A total of 5 mono-crystalline silicon PV modules were examined in the previous study. The main propose of glass coated with carbon conductive paste (contacting frame) was to provide the best conducting pathway from the active cell layer through glass to the frame and finally to the ground. In the current study, however, to better replicate the actual field conditions, only the humidity was used for the glass surface conductivity and it has much lower surface conductivity than the carbon layer used in the previous study. The following sections summarize the overall findings of this work and previous work performed at ASU-PRL.

#### 3.1 Phase-I: Positive Bias

Figure 3 illustrates the overall effect of +600V on the highly conducting carbon coated modules (previous study; mf1) and on the mildly conducting 85%RH water layered modules (present study; mf2, mf3). This figure clearly indicates that there is little or no power loss on the positive voltage stressed modules irrespective of the type of surface conductivity (carbon layer or water layer) and pre-history (fresh, TC-stressed or DH-stressed).

![Figure 3: Absence of PID Effect at positive voltage stress irrespective of surface conductivity type (carbon or water) and pre-history (fresh, DH-stressed or TC-stressed).](image-url)

As shown in Figure 4, the extent of charge (coulombs) passing through the module varies depending on the pre-history (TC, DH or fresh) of the module but there is no significant sign of power change or degradation observed in all the seven rounds (5 hours each round) of the stress at +600V (85°C/85%RH).
3.2 Phase-II: Negative Bias

Figure 5 illustrates the power remaining in the modules after a negative-voltage stress. This figure indicates that the modules with carbon coating on glass degraded dramatically (more than 90% for the DH and fresh modules and about 82% for the TC module) within about 5 hours of stress (previous study; mf1) whereas modules stressed with humidity (current study; mf2, mf4) degraded only about 40%, 30-50% and 0% for the DH, fresh and TC modules, respectively, even after 35 hours of stress. These results clearly indicate that the performance degradation of negative-voltage stressed modules depends on the pre-history (fresh, TC-stressed or DH-stressed) and surface conductivity (conductive carbon or humidity) of the modules. It is important to note that the TC-stressed module does not seem to degrade under low surface conductivity (humidity) as compared to fresh and DH-stressed modules. It may be possible that the high temperature of the thermal cycling test might have helped curing EVA or might have driven out the moisture from the laminate and prevents or reduces modules from deterioration if the surface conductivity is very low as in the field; the humidity-based test method utilized in this work is expected to better replicate the field operation as compared to the carbon-based method. Further investigation with higher sample size from a large number of manufacturers is needed to further understand and confirm the unusual results obtained with the TC-stressed modules of this investigation.

As shown in Figure 6, the coulombs passing through the module varies depending on the pre-history of the module. The amount of coulombs transferred through the fresh module is about 2 times higher than through the DH or TC module; however, the power degradation level is drastically different from one module to the other. The DH and fresh modules experienced a power drop of 40-50% whereas the TC module did not experience any power drop at all. In other words, the power drop in DH module is about 40% whereas the power drop in TC module is practically zero though both modules experienced nearly the same coulomb transfer.

3.3 Phase-III: Regeneration/Recovery Bias

Degraded modules after negative bias can be fully or partially recovered by applying positive bias; this method is here called as regeneration/recovery bias. As indicated in Figure 5, the power degradation of carbon-coated samples under negative voltage stress for 5 hours is more than 90% for the DH and fresh modules, and is about 82% for the TC module. As shown in Figure 7, during the recovery process of the carbon-based samples with positive voltage for the same 5 hours, the full recovery could not be obtained. However, as shown in Figure 8, a full recovery of the humidity-based samples could be obtained during the same recovery time (35 hours; Figure 7) as that of the stress time (35 hours; Figure 5). For the same stress and recovery duration, the reason for only the partial recovery of the
carbon-based samples and for the full recovery of the humidity-based samples is not clear.

Figure 7: Performance recovery at positive voltage stress depending on the surface conductivity type (carbon-partial recovery; humid-full recovery)

Figure 8: Fraction of power remaining vs. Total coulombs transferred in mf4 with recovery bias of +600 V (1 round is equal to 5 hours)

Figure 9 provides an overview on the electroluminescence (EL) images of the modules that underwent negative-voltage stress in this study (water as surface conductive layer as opposed to carbon layer). In the previous study it was observed that all the cells in the module degrade uniformly throughout the module (both edge and center cells) due to high conductivity of carbon throughout the glass surface [1]. The EL images shown in Figure 9 indicate that only the edge cells close to the frame of fresh and DH-stressed modules experience higher inactive areas (higher degradation) as compared to the cells at the center. From this study, it may be stated that the water-layer (humidity) method may be more appropriate to simulate the field degradation (if any) pattern as compared to the metallic/carbon conductive layer. The metallic/carbon conductive layer method may still be used for quick screening of c-Si cells for PID susceptibility as it requires only very short sample preparation time and a simple test setup.

IV. CONCLUSIONS

Irrespective of PID test temperature (85°C or 60°C) and pre-history (fresh or pre-stressed in damp-heat or thermal-cycling), this study indicates that the positive-voltage has little or no PID effect on all the tested modules when humidity or carbon is used for the glass surface conductivity. In contrast, irrespective of PID test temperature (85°C or 60°C) and pre-history (fresh or pre-stressed in damp-heat or thermal-cycling), all the tested modules appear to be susceptible to the negative-voltage when conductive carbon (carbon layer) is used for the glass surface conductivity. However, when humidity is used for the surface conductivity instead of carbon, only the fresh and damp-heat stressed modules, excluding thermal-cycling stressed modules, appear to be susceptible to the negative voltage irrespective of PID test temperature (85°C or 60°C). Based on the EL studies performed in the previous and current studies, it may be stated that the humidity based method better replicates the field degradation (if any) as compared to the metallic/carbon conductive layer. The metallic/carbon conductive layer method may still be used for quick screening of c-Si cells for PID susceptibility as it requires only very short sample preparation time and a simple test setup.

REFERENCES


Figure 1: Experimental Setup used for PID Evaluations at ASU-PRL
Figure 2: Flow Diagram of Overall Test Program with Voltage Stress and Characterization at 5h Intervals (Either 5 or 4 modules per project were used leading to a total of 18 modules)

Figure 9: Images of Electroluminescence before PID, during PID (-600V) and Recovery (+600V) Stages

Cells Shunting